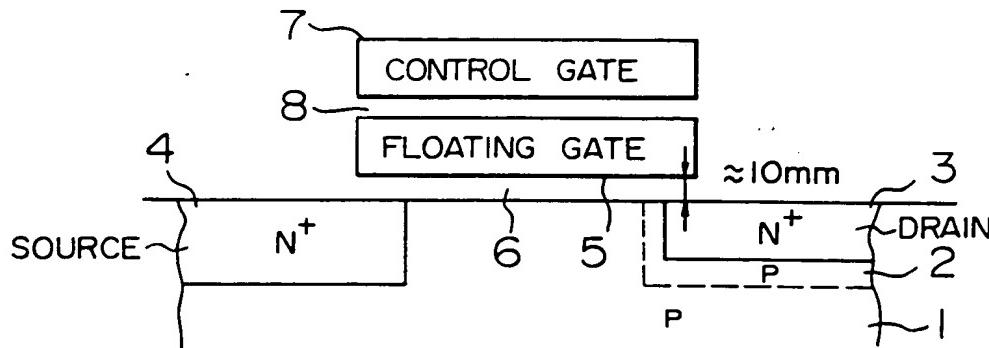
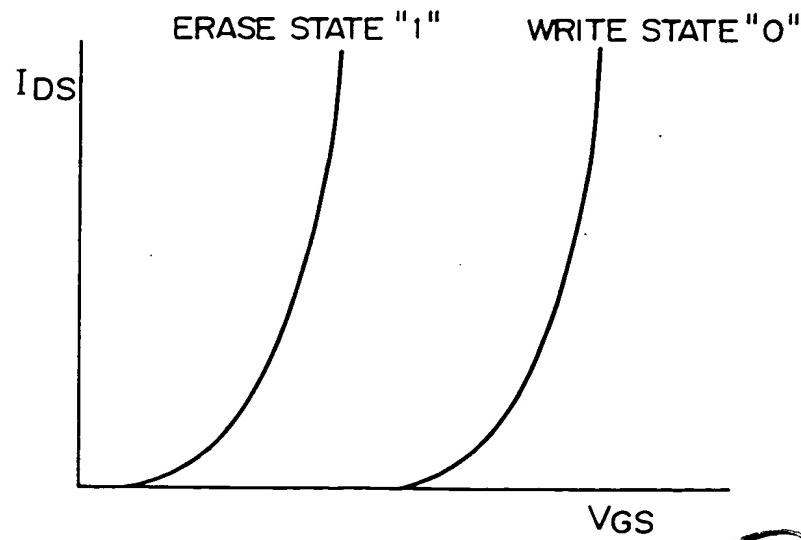


APPROVED BY DRAFTSMAN	O.G. FIG. CLASS	SUBCLASS
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**F I G. 1A**



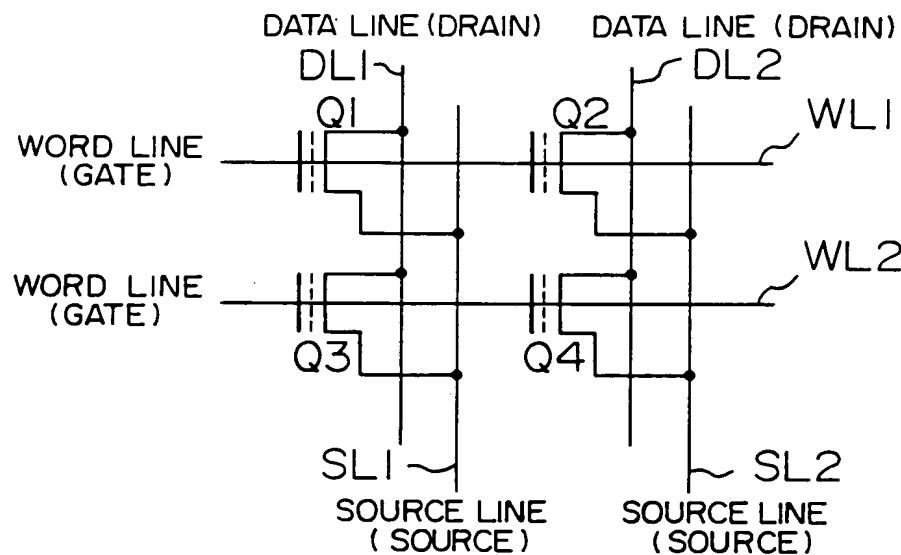
**F I G. 1B**



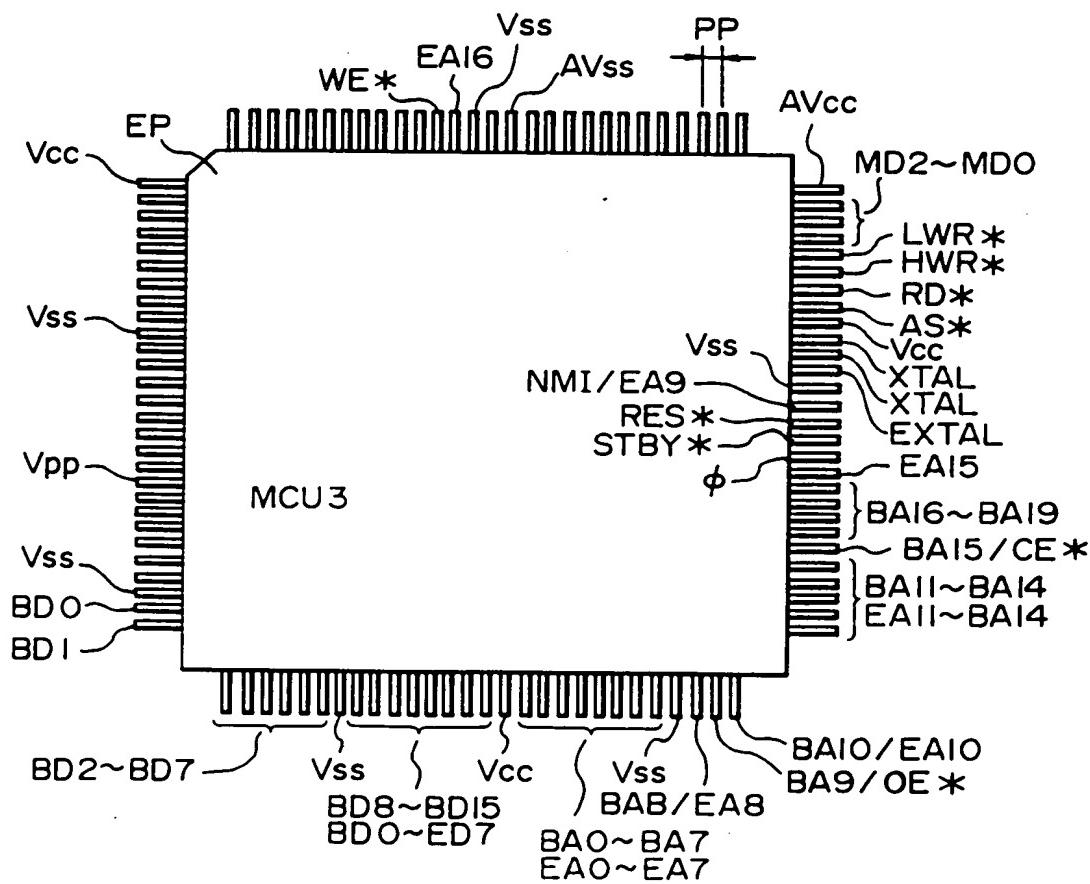
(40)

APPROVED BY CRAFTSMAN	O.G. FIG. CLASS SUBCLASS
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**F I G. 2**

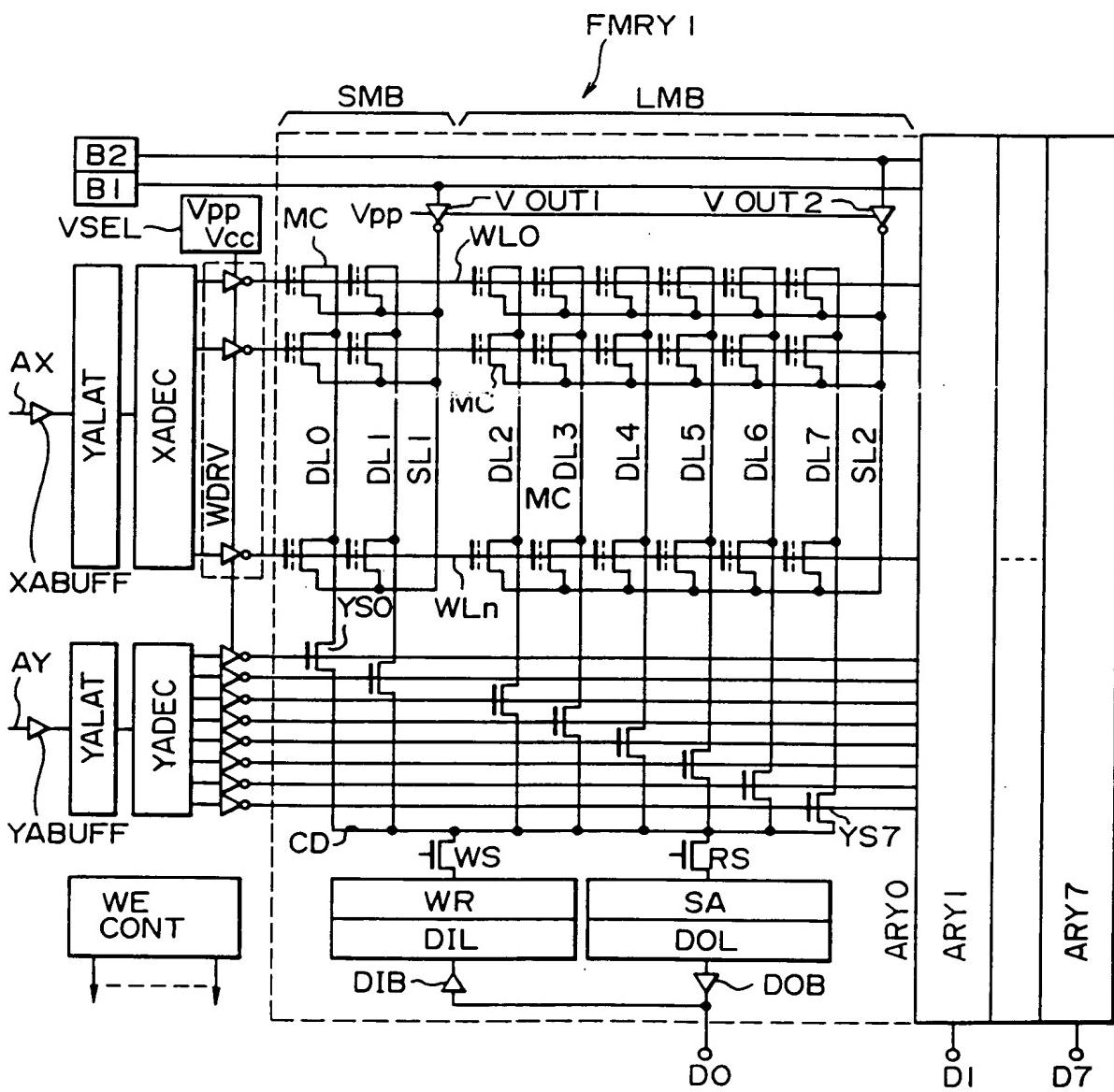


**F I G. 9**



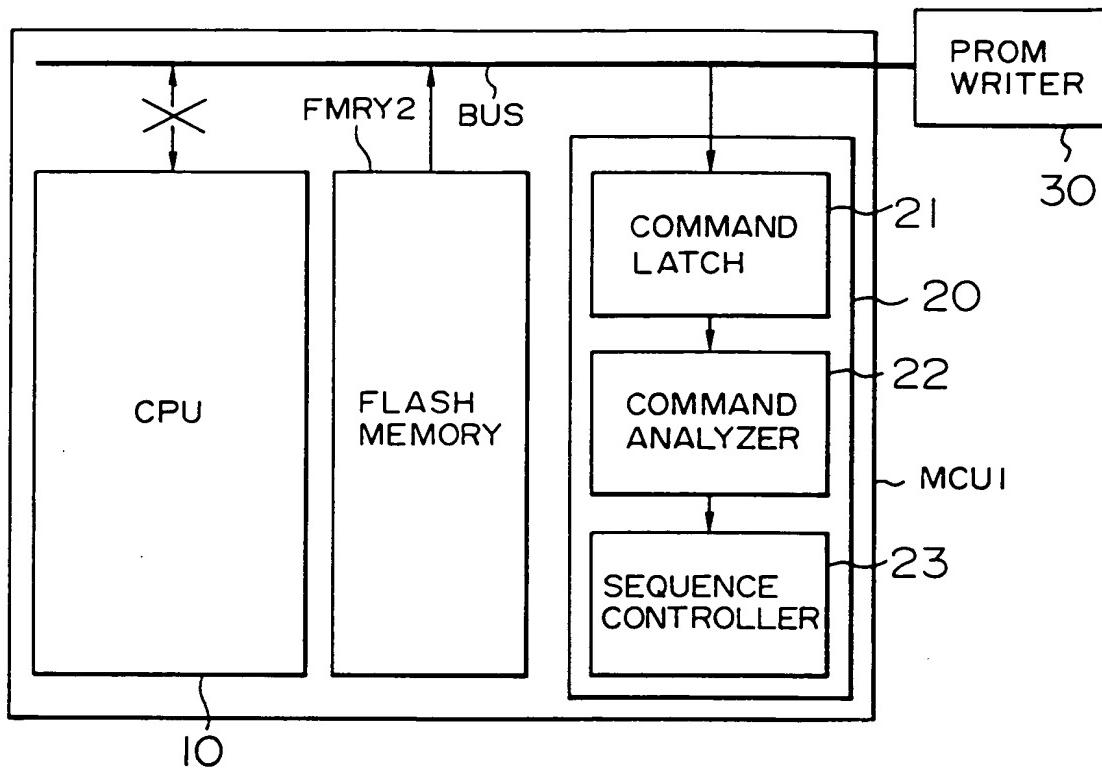
APPROVED	O.G. FIG.
BY	CLASS SUBCLASS
DRAFTSMAN	

FIG. 3

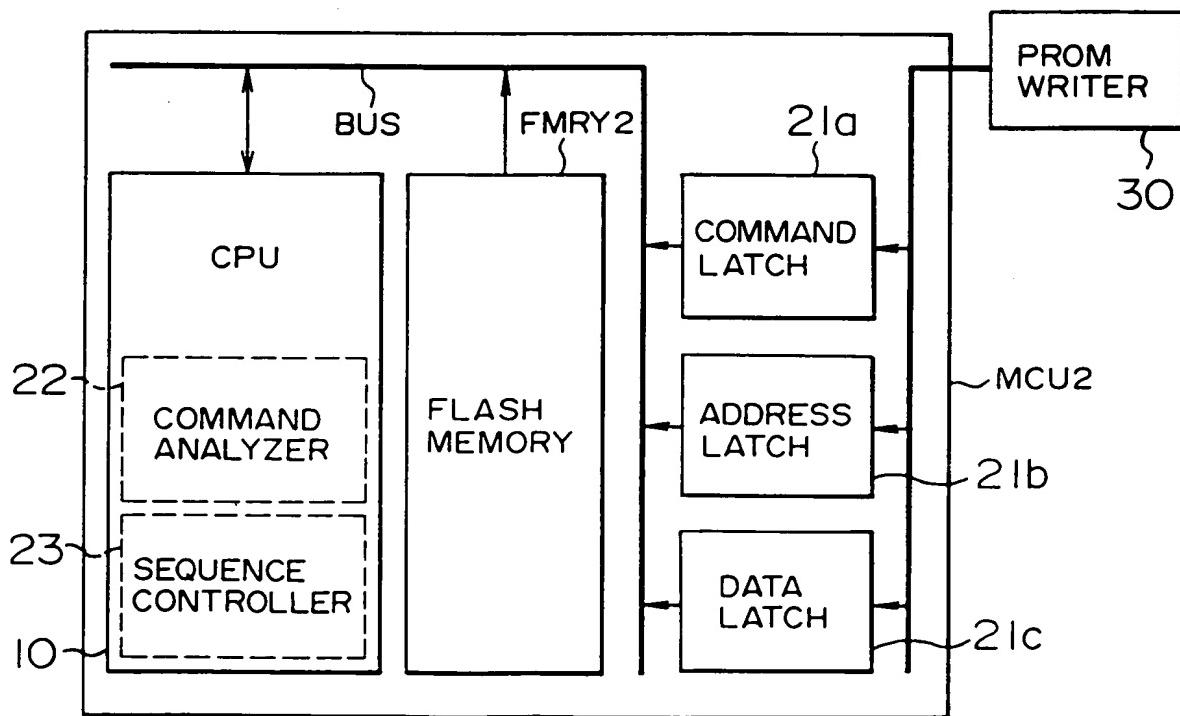


APPROVED BY CRAFTSMAN	O.G. FIG. CLASS      SUBCLASS
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**F I G. 4**



**F I G. 5**



APPROVED	O.G. FIG.
BY	CLASS SUBCLASS
DRAFTSMAN	

FIG. 6A

ADDRESS

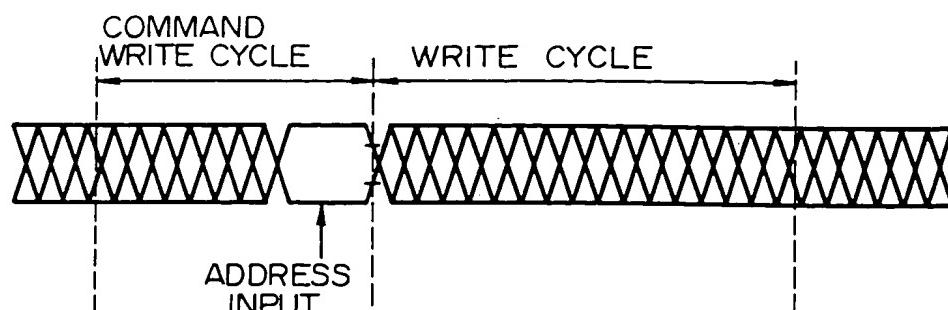


FIG. 6B

WRITE SIGNAL

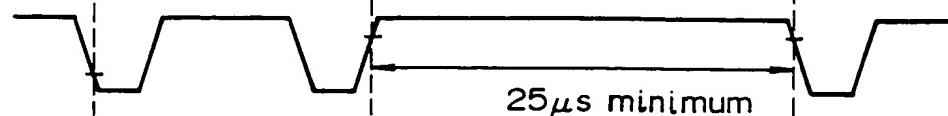


FIG. 6C

DATA

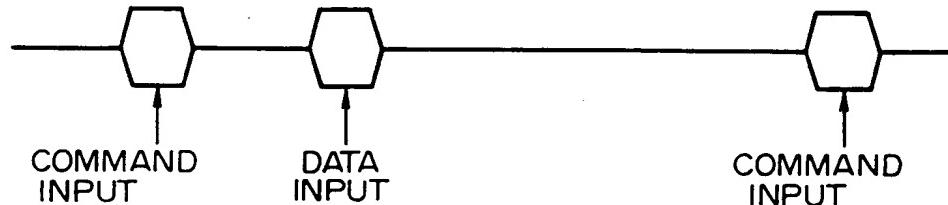


FIG. 7

WRITE SIGNAL

WRITE CYCLE

DATA

CPU OPERATION

COMMAND ANALYSIS

WRITE

POST-PROCESSING

5.7 μs

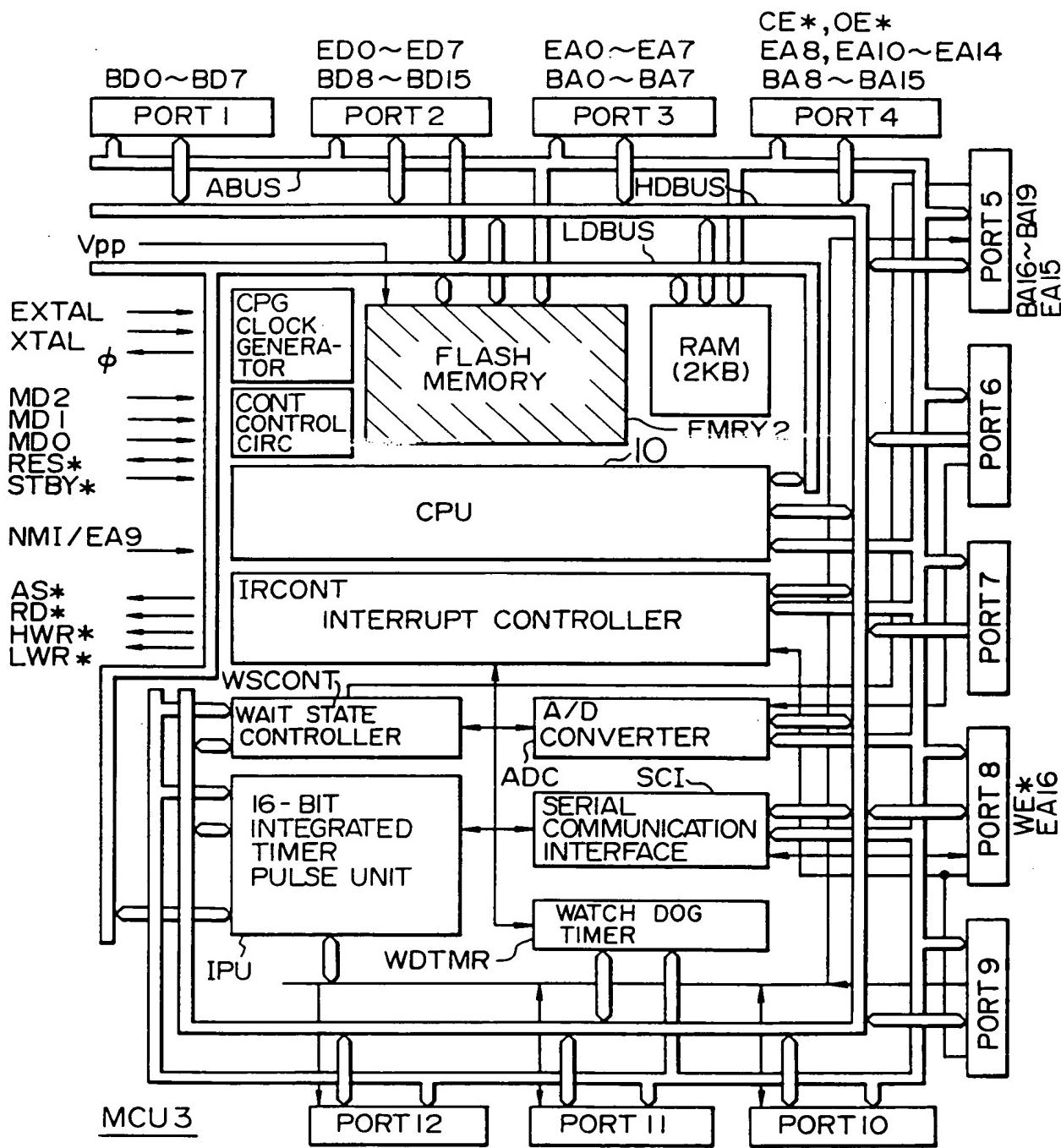
18.1 μs

1.2 μs

25μs minimum

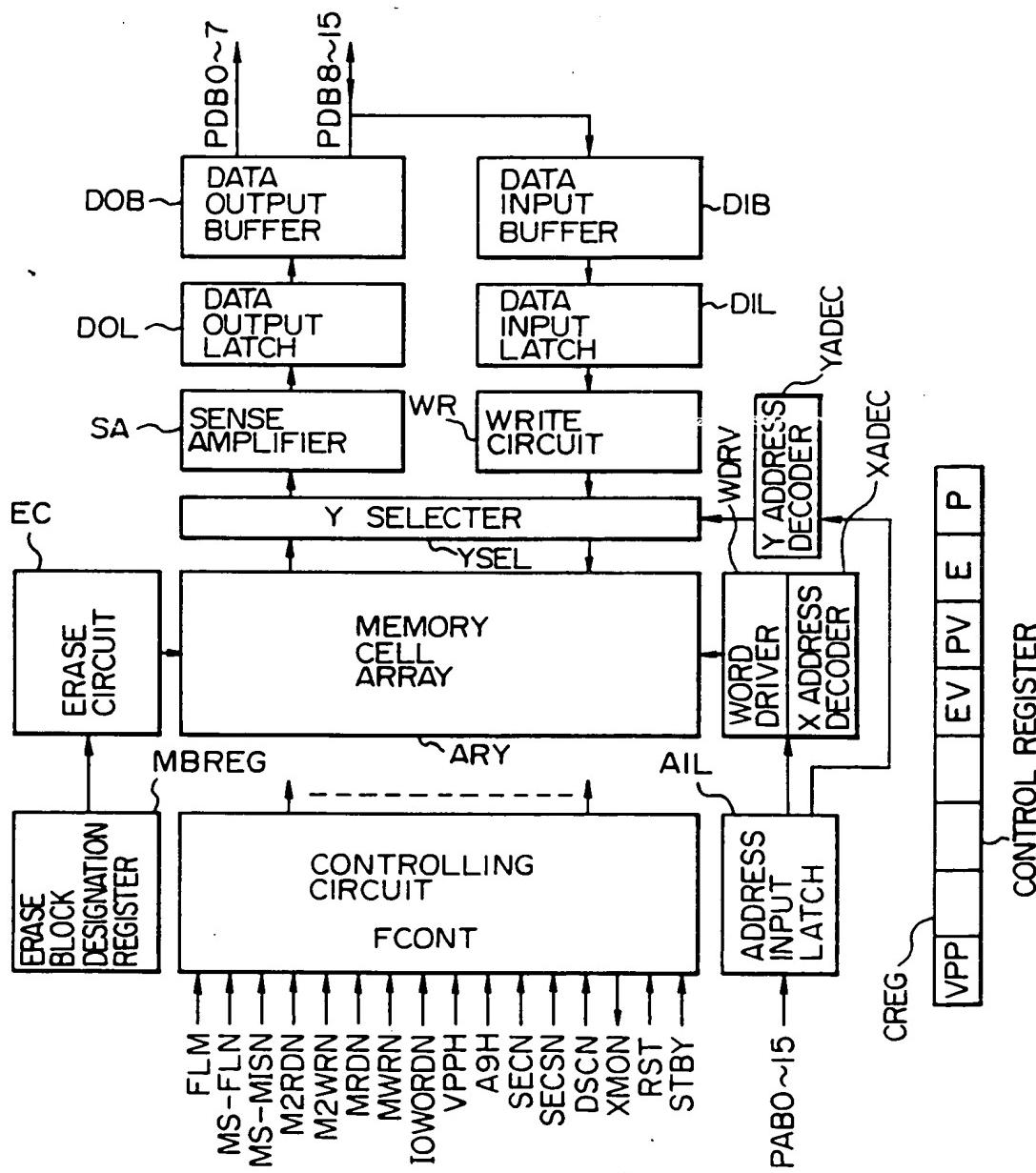
APPROVED	O.G. FIG.
BY	CLASS SUBCLASS
DRAFTSMAN	

FIG. 8



APPROVED BY CRAFTSMAN	O.G. FIG. CLASS      SUBCLASS
-----------------------------	----------------------------------

FIG. 10



APPROVED BY DRAFTSMAN	O.G. FIG. CLASS	SUBCLASS
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FIG. 11

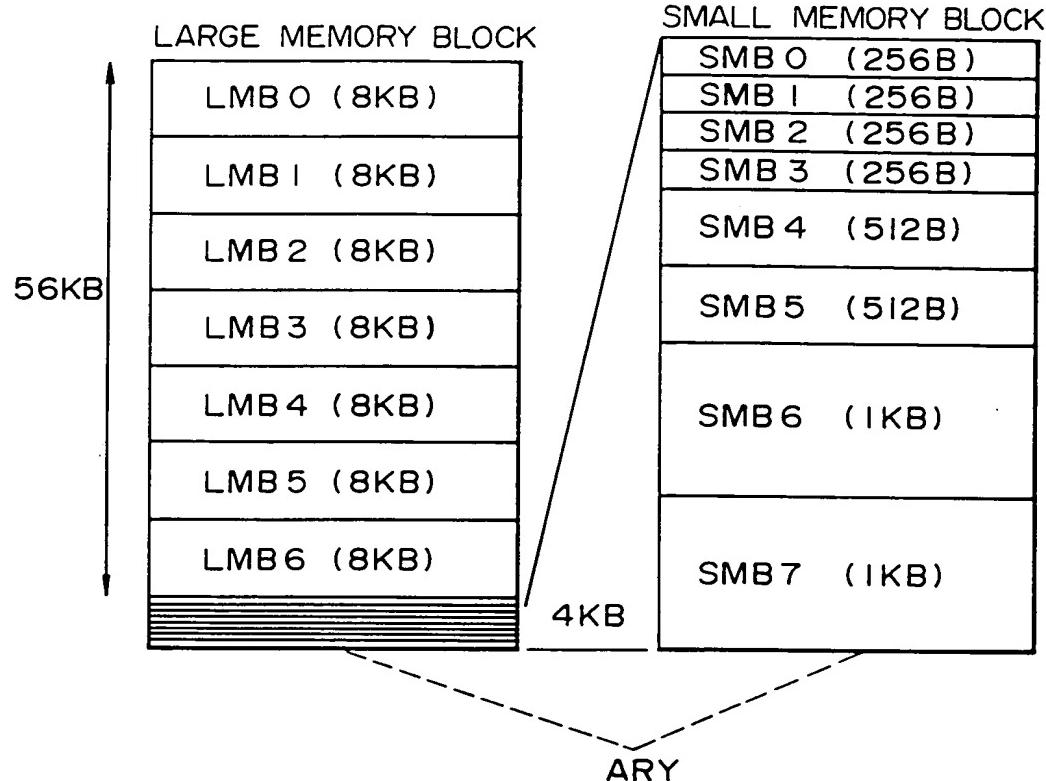
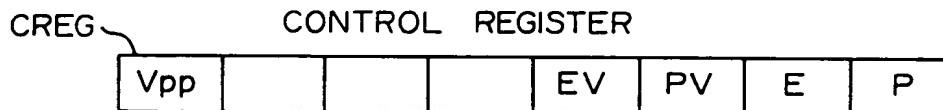


FIG. 12A



Vpp Vpp APPLICATION FLAG

EV ERASE VERIFY FLAG

PV PROGRAM VERIFY FLAG

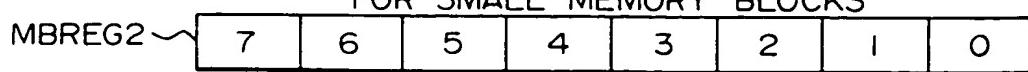
E ERASE FLAG

P PROGRAM FLAG

FIG. 12B ERASE BLOCK DESIGNATION REGISTER FOR LARGE MEMORY BLOCKS

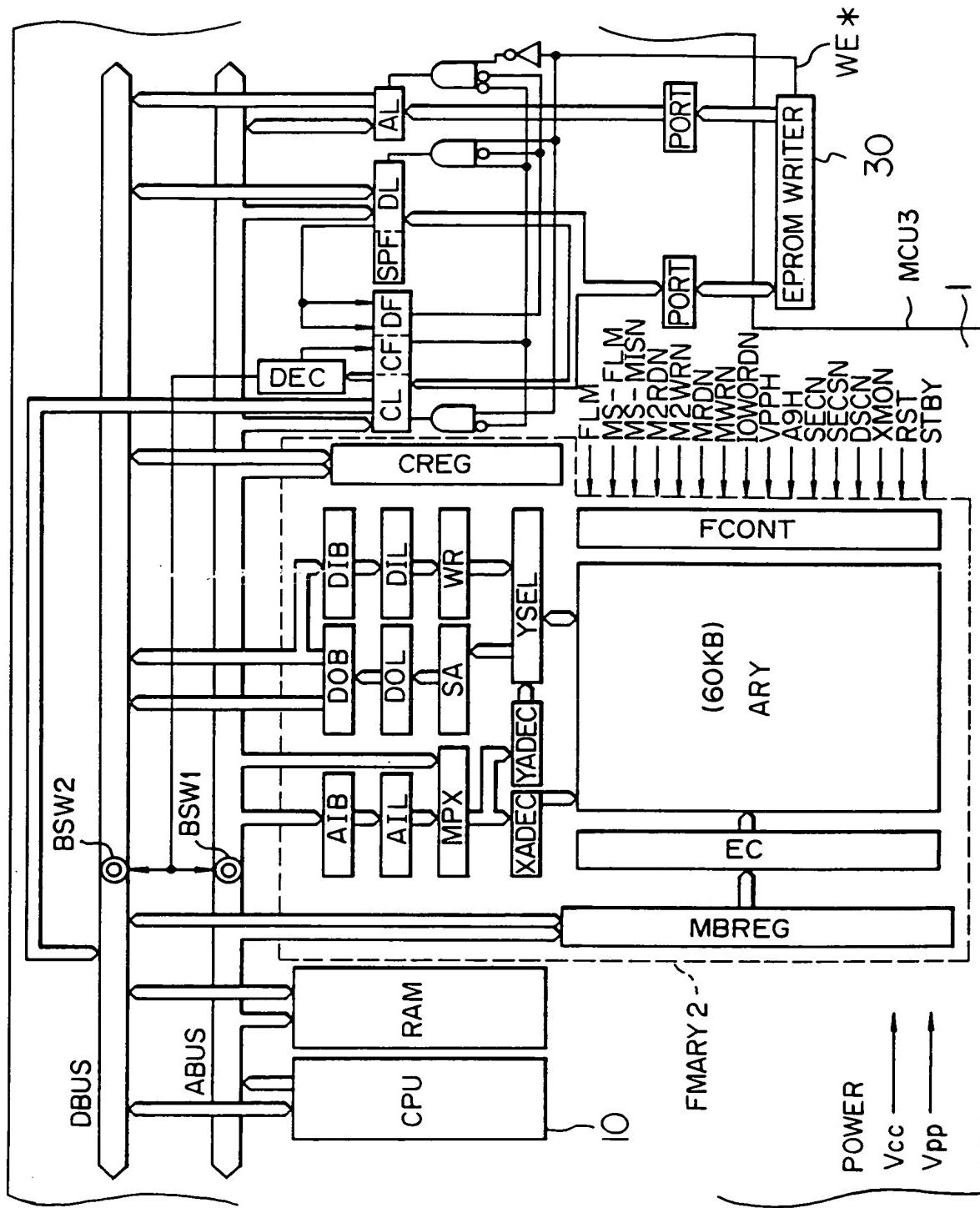


FIG. 12C ERASE BLOCK DESIGNATION REGISTER FOR SMALL MEMORY BLOCKS



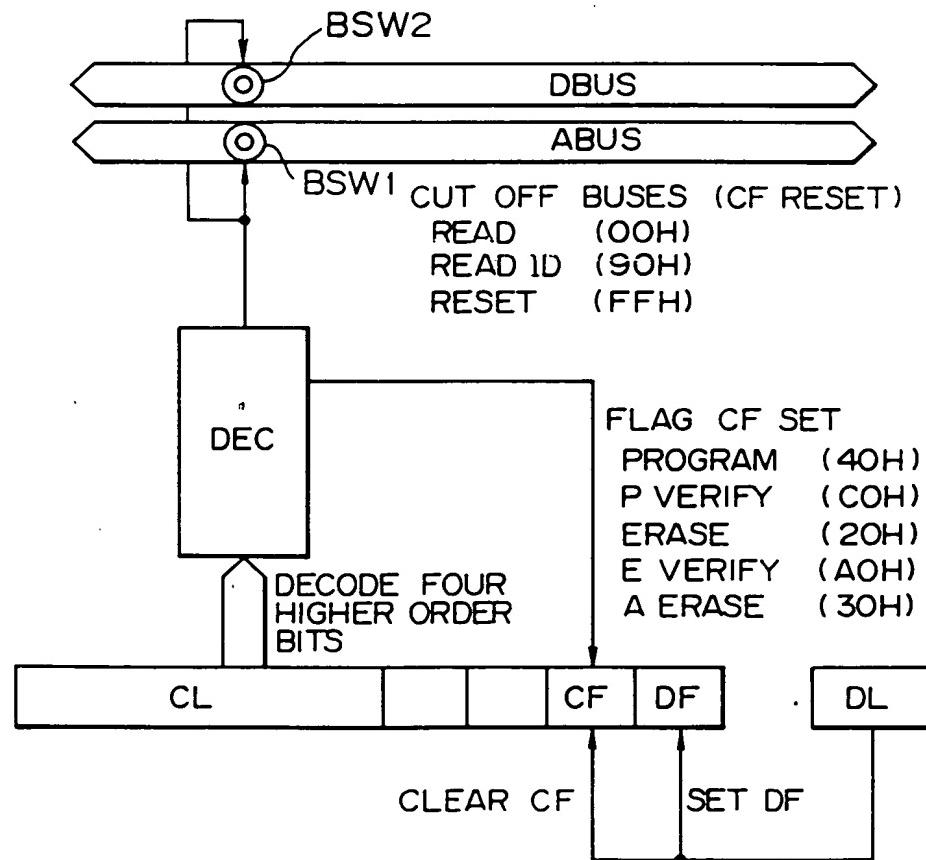
APPROVED BY  DRAFTSMAN	O.G. FIG. CLASS      SUBCLASS
---------------------------------	----------------------------------

FIG. 13



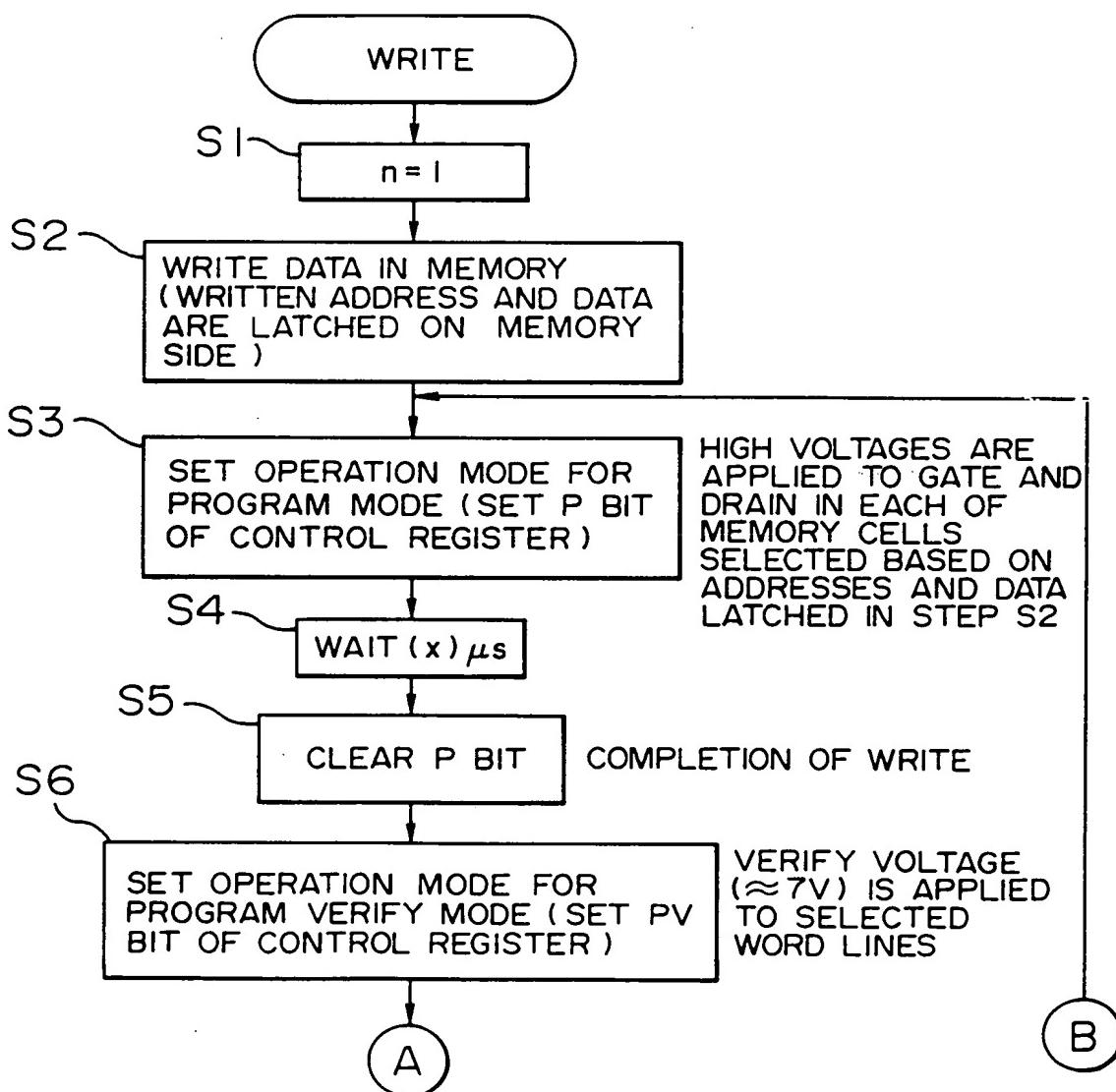
APPROVED	O.G. FIG.
BY	CLASS SUBCLASS
DRAFTSMAN	

FIG. 14



APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
RAFTSMAN		

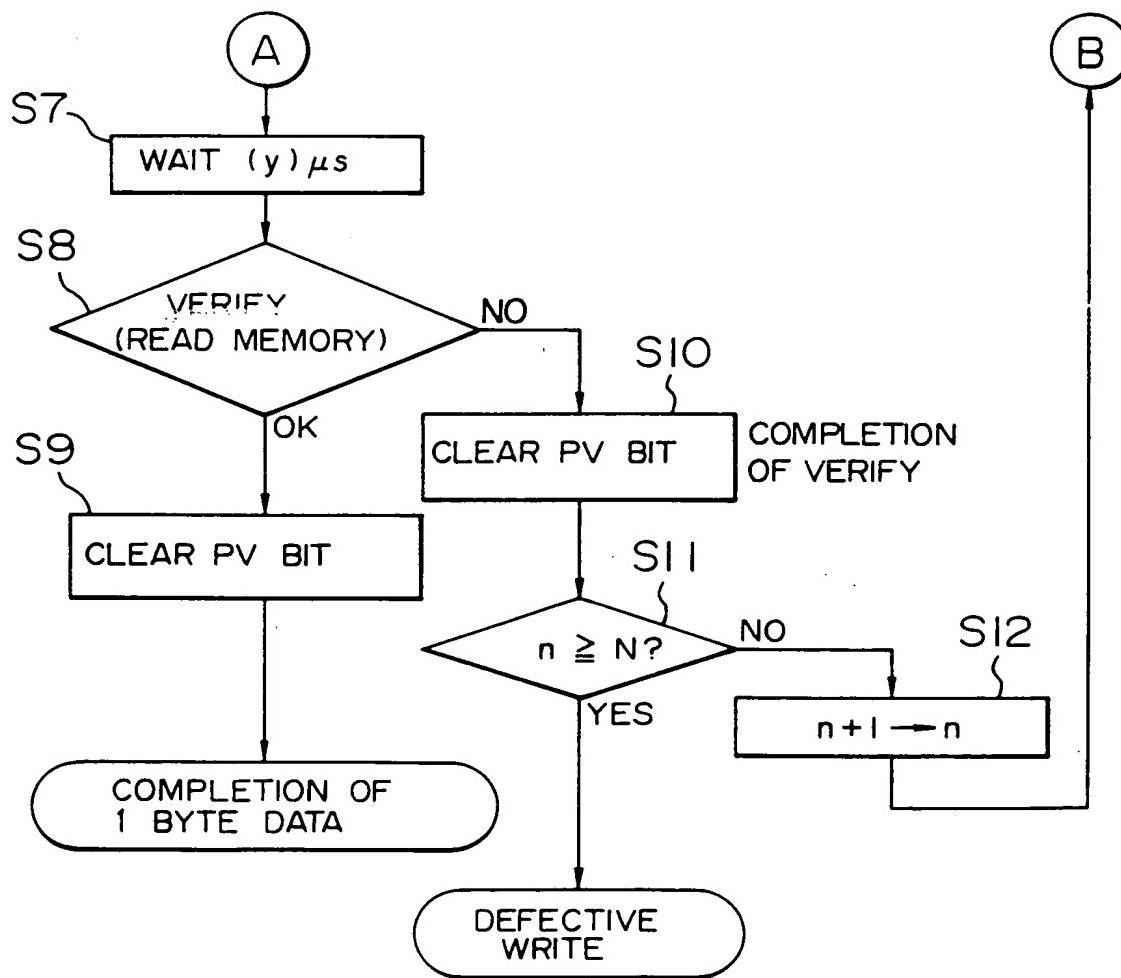
FIG. 15A



00000000-0000-0000-0000-000000000000

APPROVED BY CRAFTSMAN	O.G. FIG. CLASS	SUBCLASS
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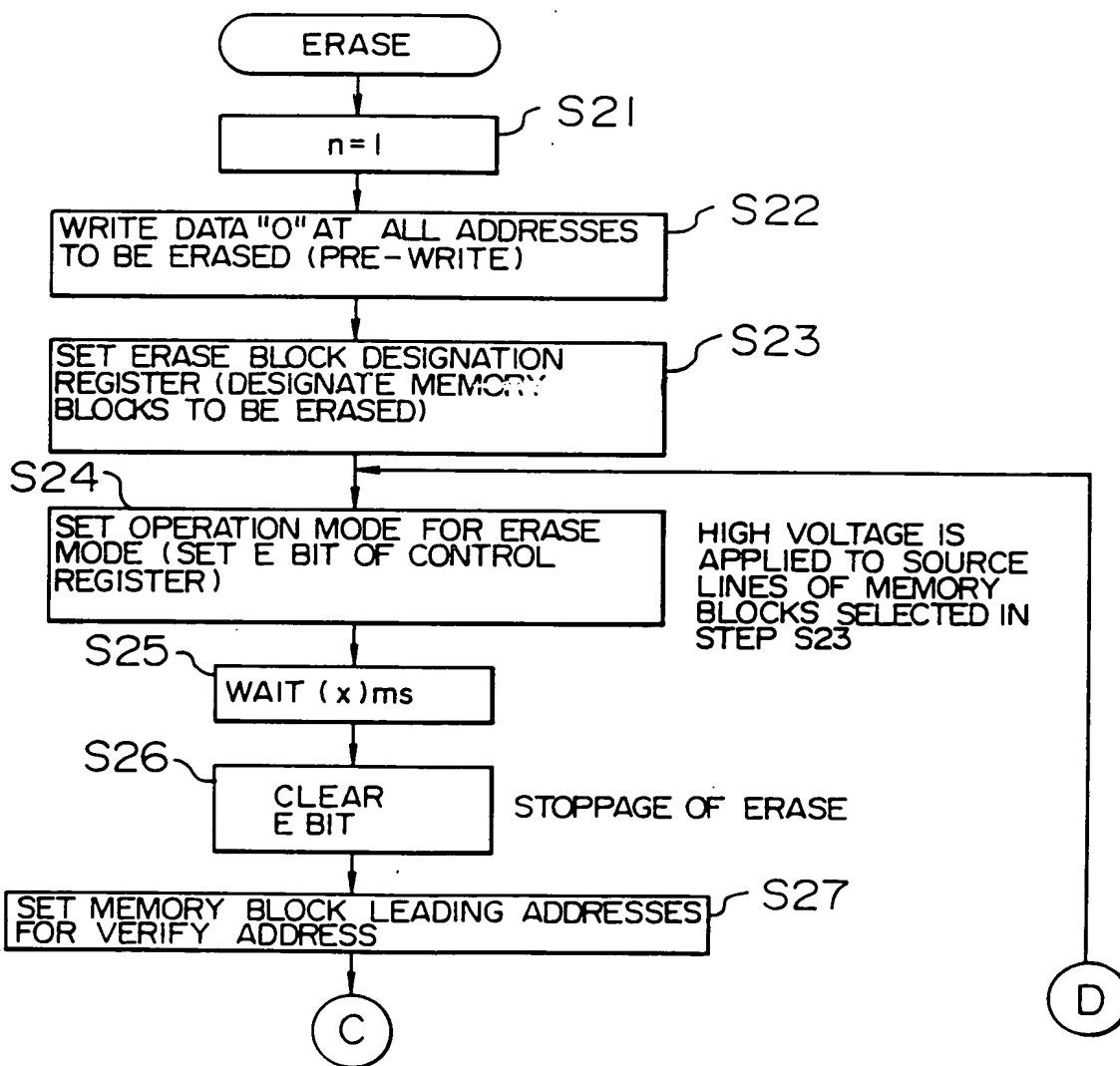
F I G. 15 B



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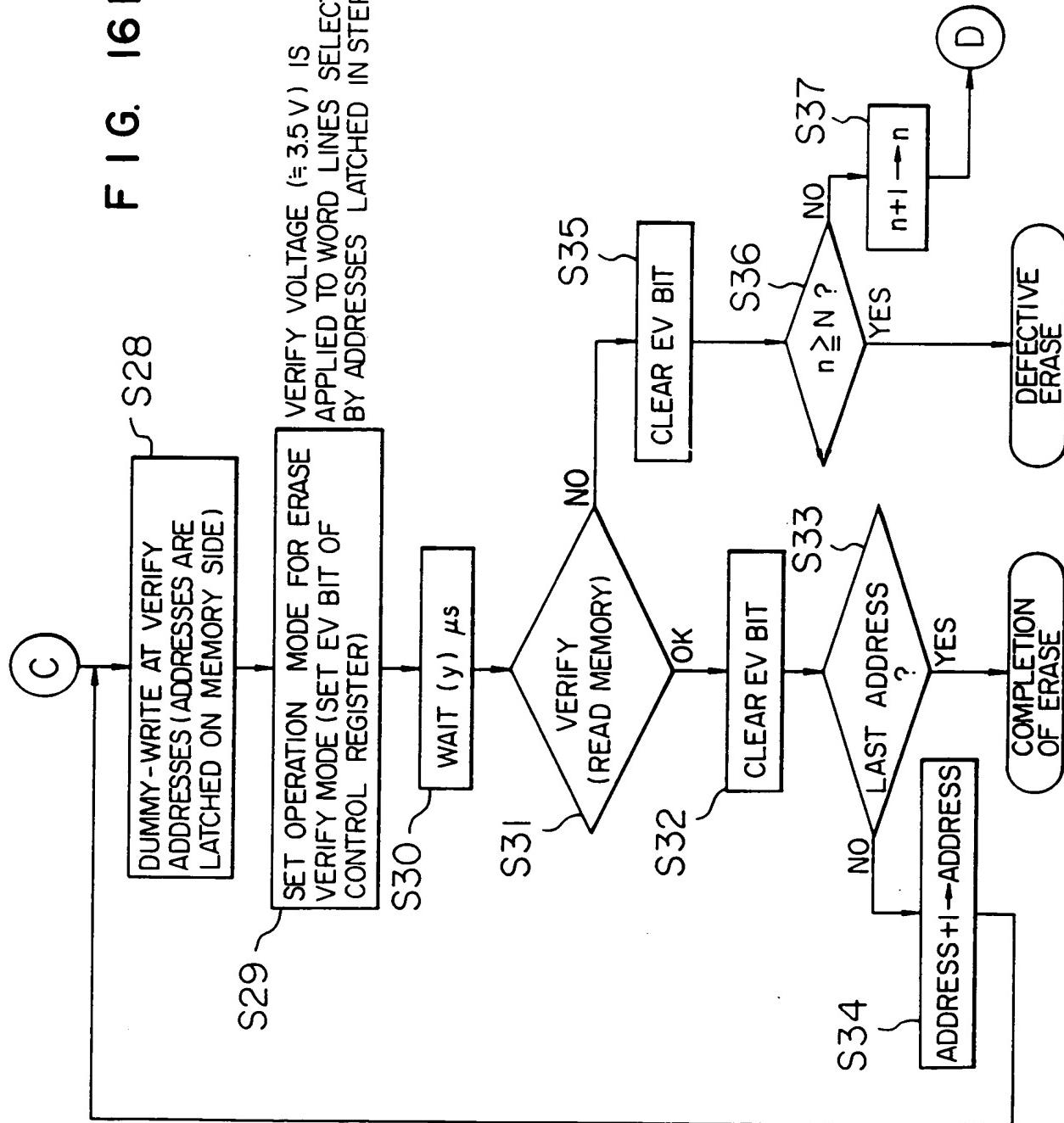
APPROVED BY DRAFTSMAN	O.G. FIG. CLASS	SUBCLASS
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F I G. 16 A



APPROVED	O.G. FIG.
BY	CLASS SUBCLASS
STGMAN	

**F I G. 16 B**



APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

## FIG. 17

WRITE  
("PROGRAM")

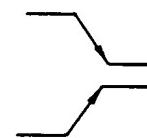
ADDRESS IS ALWAYS LATCHED  
AT FALL OF WE\* REGARDLESS  
OF FLAG STATES

FLAG STATE

WE\*

CF DF

0 0



ADDRESS IS LATCHED  
(DON'T CARE)

0 0

COMMAND IS LATCHED IN CL  
COMMAND IS DECODED  
BY DECODER

\*BUSES : KEPT CONNECTED  
\*CF : "0" → "1"

1 0

ADDRESS IS LATCHED

1 0

DATA IS LATCHED IN DL

\*CF : "1" → "0"

\*DF : "0" → "1"

### OPERATION OF CPU

- POLLING OF FLAGS

READ COMMAND FROM CL IN  
CF = 1 STATE (COMMAND IS STORED IN CL BUT NO DATA  
IS STORED IN DL) OR  
DF = 1 STATE (DATA HAS ALREADY BEEN STORED IN DL)

- ANALYSIS OF COMMAND

TRANSFER ADDRESS AND DATA TO AL AND DL,  
RESPECTIVELY

SET P BIT OF CONTROL REGISTER

- WAIT ( $x$ )  $\mu$ s

CLEAR P BIT OF CONTROL REGISTER

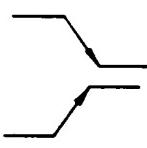
- DF = 0

0043220255-02242006

APPROVED	O.G. FIG.
BY	CLASS SUBCLASS
FETSMAN	

## FIG. 18

WRITE VERIFY ("P VERIFY")

FLAG STATE	WE*	
C F      D F		ADDRESS IS LATCHED ( DON'T CARE )
O      O		COMMAND IS LATCHED IN CL COMMAND IS DECODED BY DECODER

\*BUSES : KEPT CONNECTED  
\*CF : "O" → "I"

---

OPERATION OF CPU

- POLLING OF FLAGS  
READ COMMAND FROM CL IN  
C F = 1 STATE ( COMMAND IS STORED IN CL BUT NO DATA IS STORED IN DL ) OR  
D F = 1 STATE ( DATA HAS BEEN STORED IN DL )
- ANALYSIS OF COMMAND  
PV BIT OF CONTROL REGISTER IS SET  
READ DATA AT ADDRESS FOR WRITING BY USE OF THE ADDRESS FOR WRITING ( STORED BY CPU )  
CLEAR PV BIT OF CONTROL REGISTER
- C F = "I" → "O"

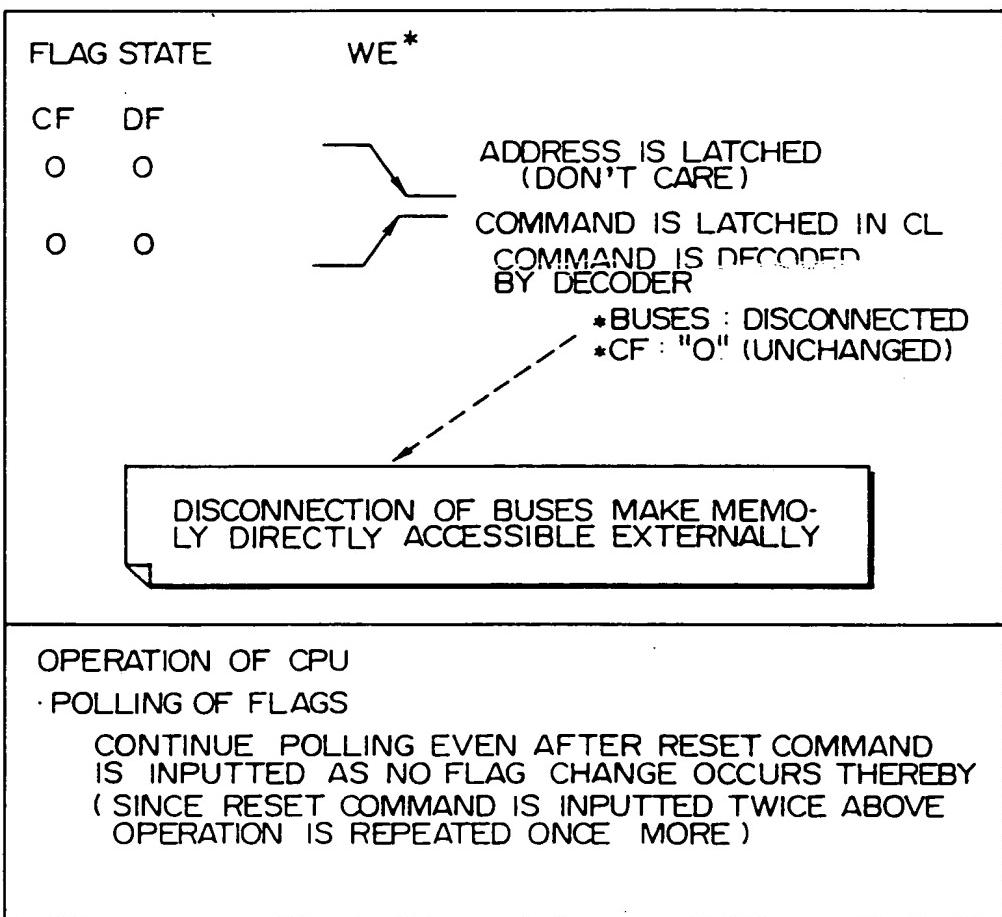
09332085 - 09342086

APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

## FIG. 19A

RESET ("RESET")

(1) WHEN RESET COMMAND IS FIRST INPUTTED



APPROVED BY	O.G. FIG.
	CLASS SUBCLASS
DRAFTSMAN	

## F I G. 19 B

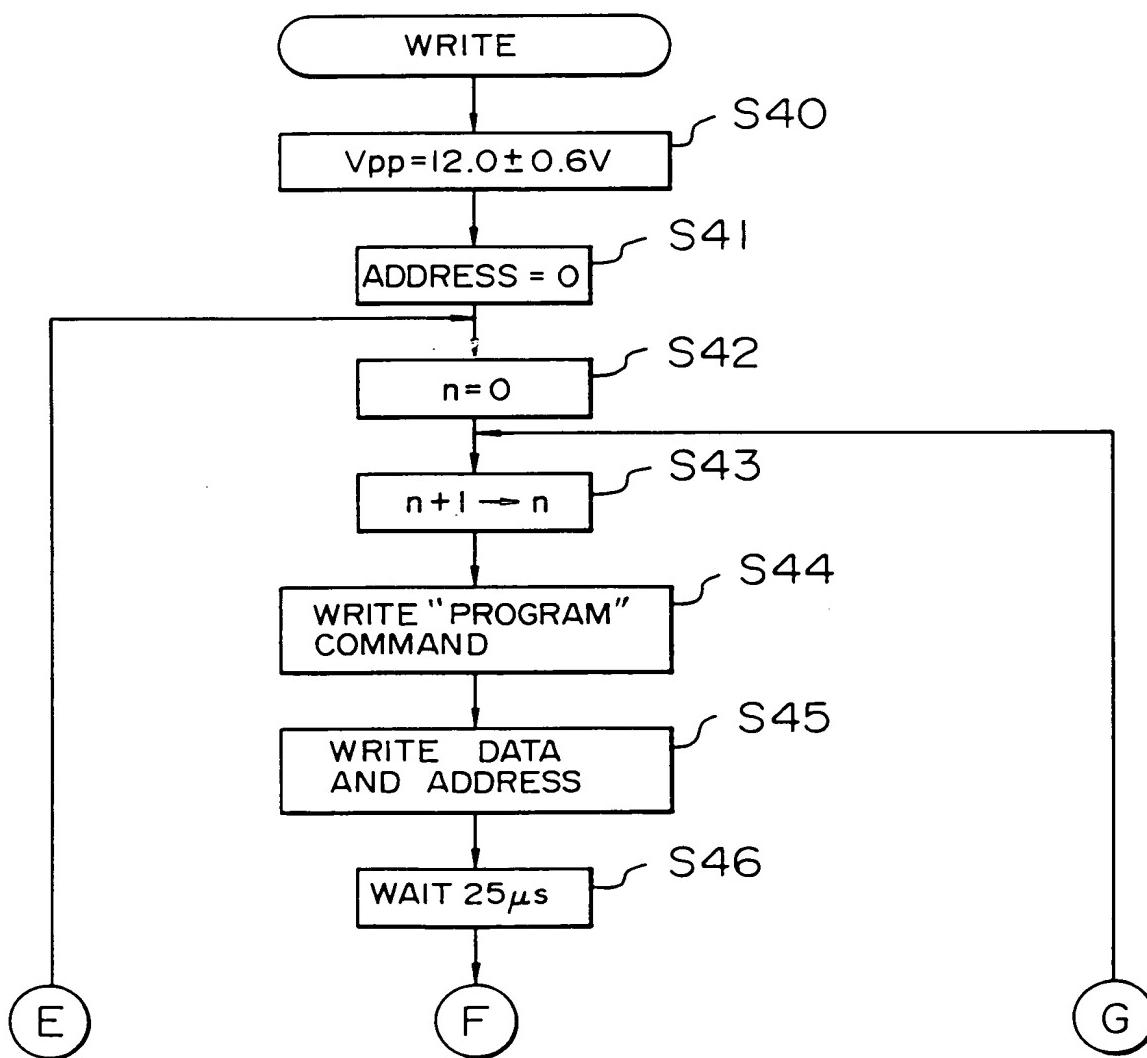
RESET ("RESET")

(2) WHEN RESET COMMAND IS INPUTTED TO INTERRUPT ANOTHER COMMAND

FLAG STATE	WE*	
C F      D F		
I            O		ADDRESS IS LATCHED ( DON' T CARE )
I            O		COMMAND IS LATCHED IN CL  * C F : "I" → "O" * D F : "O" → "I"
		( UNDER CPU OPERATION )
O            I		* D F : "I" → "O"
O            O		ADDRESS IS LATCHED COMMAND IS LATCHED IN CL
O            O		COMMAND IS DECODED BY DECODER  * BUSES : DISCONNECTED * C F : "O" ( UNCHANGED )
OPERATION OF CPU		
IF RESET COMMAND IS INPUTTED DURING WRITE MODE, "FFH" WILL BE WRITTEN AS DATA. HOWEVER, SINCE "FFH" REPRESENTS NO DATA TO BE WRITTEN, NO DATA WILL BE ACTUALLY WRITTEN.		
IF RESET COMMAND IS INPUTTED DURING ERASE MODE, ERASE OPERATION WILL BE ENDED AFTER RECOGNITION OF THE 2ND COMMAND AS NOT BEING ERASE COMMAND.		
FOR OPERATION AFTER 2ND COMMAND INPUT, ABOVE OPERATION IS FOLLOWED.		

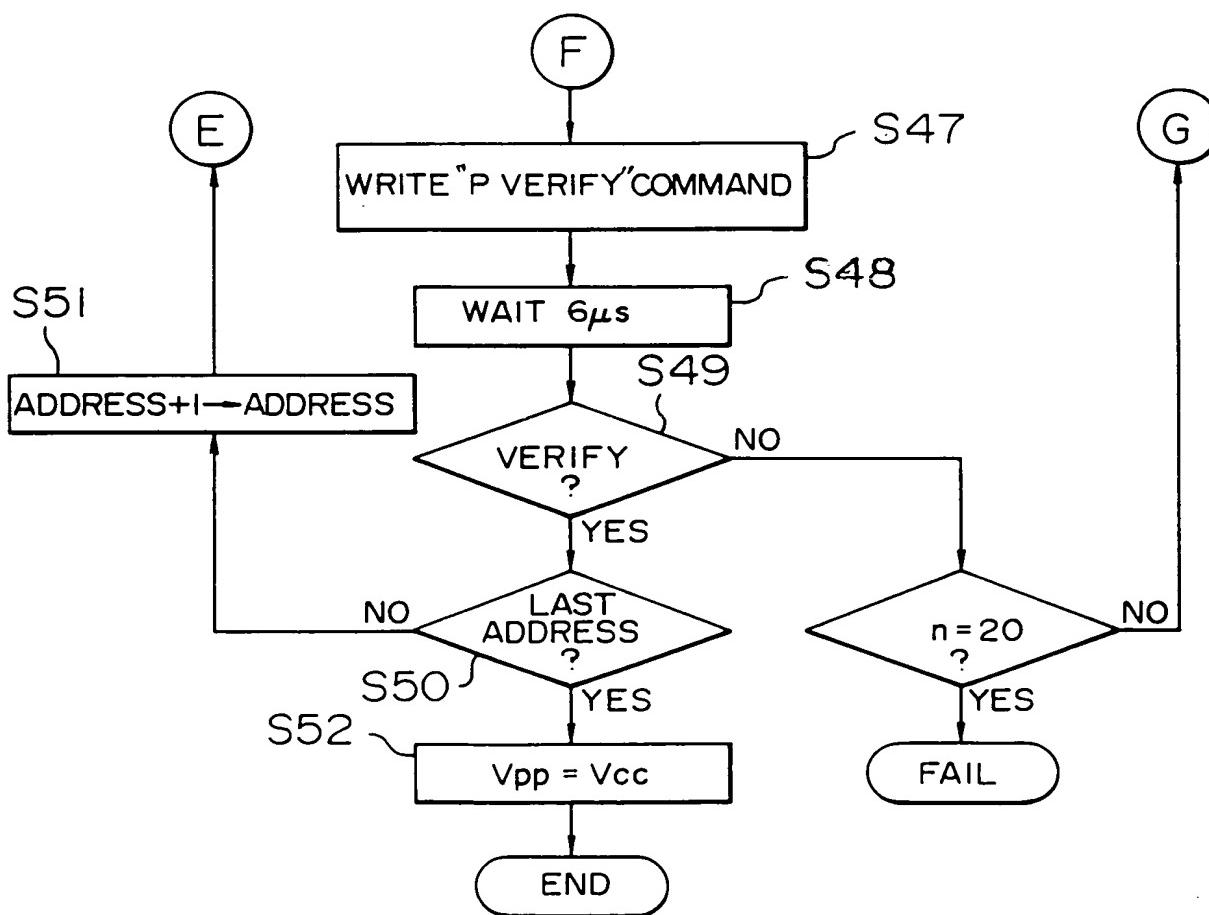
APPROVED	O.G. FIG.
BY	CLASS
DRAFTSMAN	SUBCLASS

FIG. 20A



APPROVED	O.G. FIG.	
BY	CLASS	SUBCLASS
DRAFTSMAN		

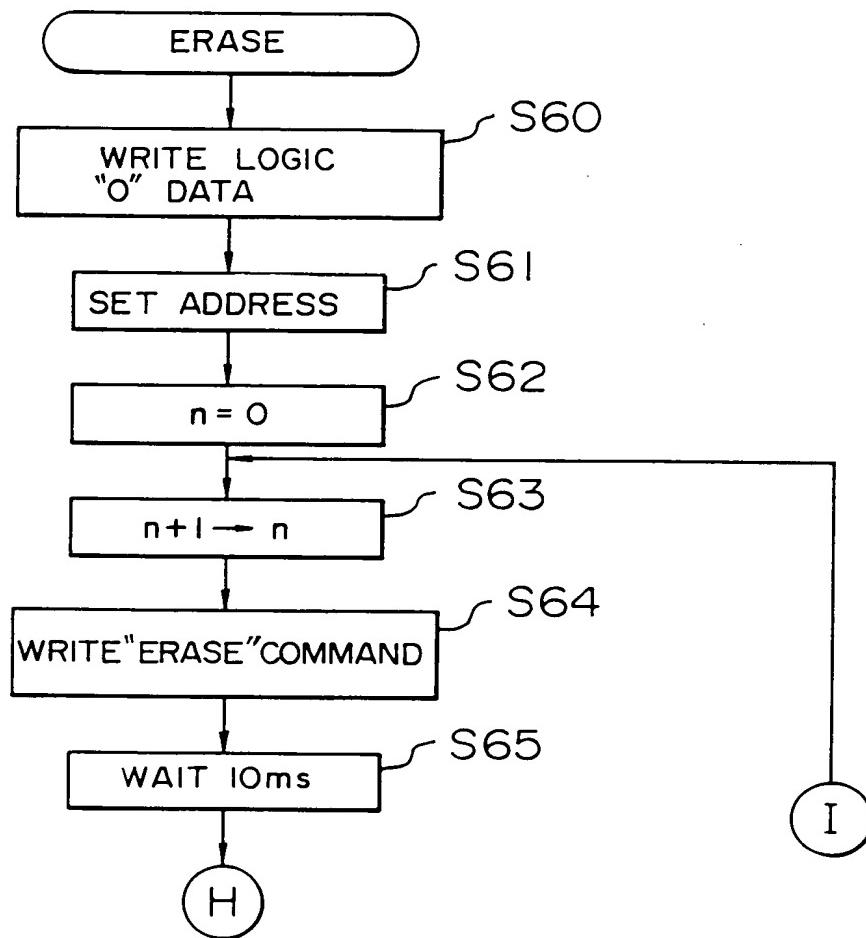
F I G. 20B



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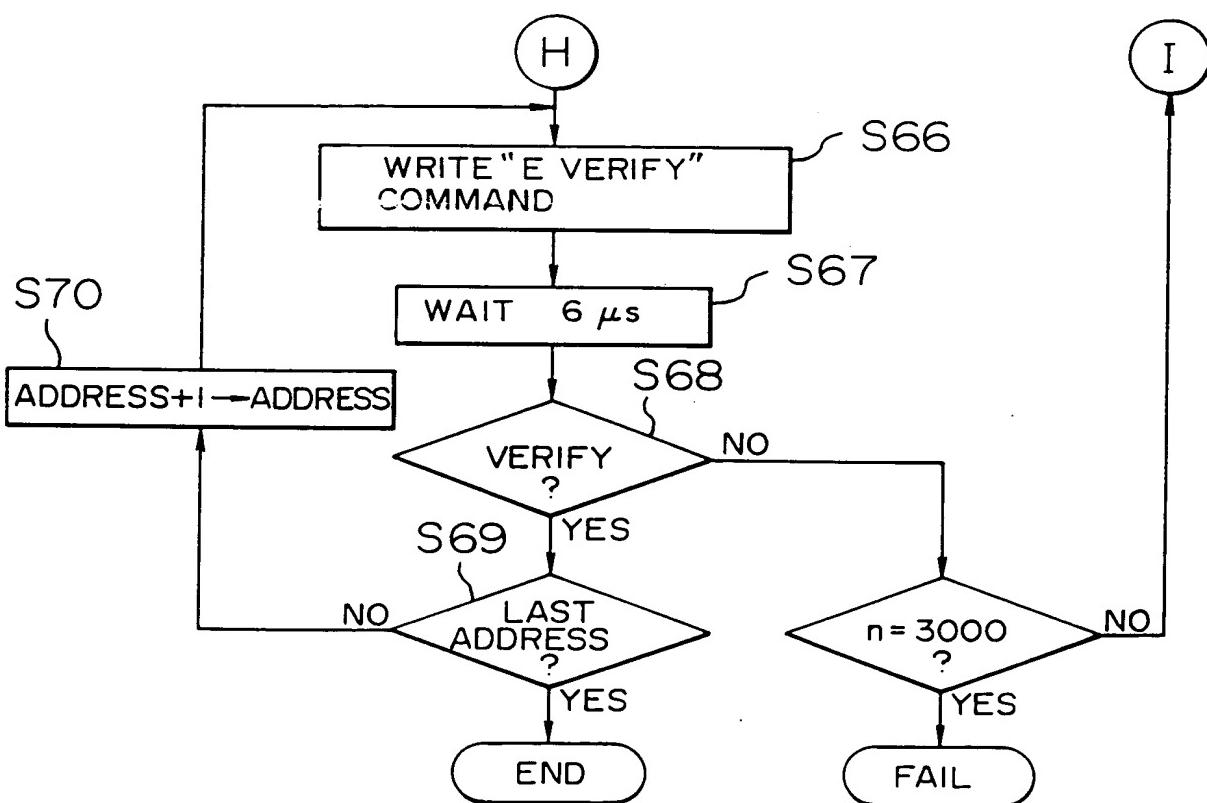
APPROVED	O.G. FIG.
BY	CLASS
DRAFTSMAN	SUBCLASS

F I G. 21A



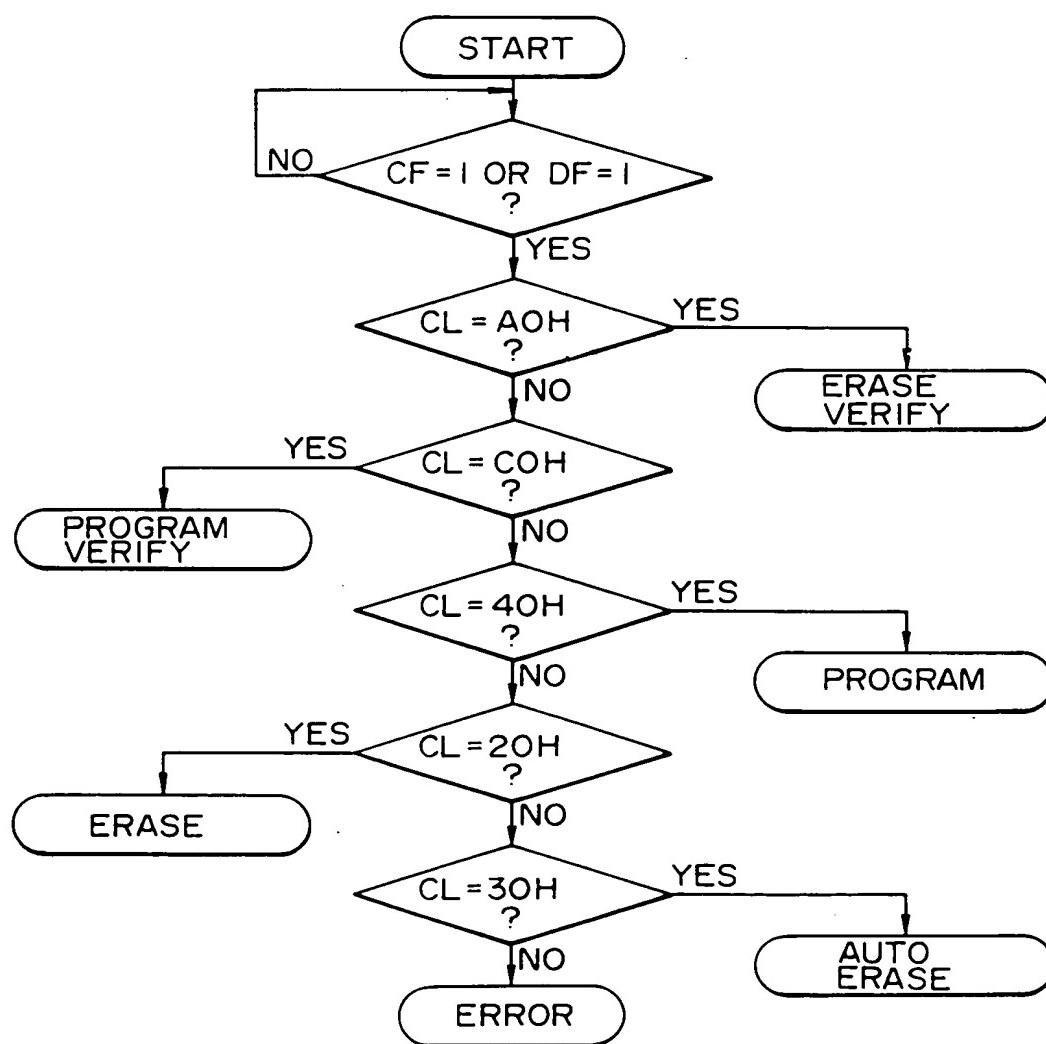
APPROVED BY	O.G. FIG. CLASS	SUBCLASS
DRAFTSMAN		

**F I G. 21 B**



APPROVED	O.G. FIG.
BY	
DRAFTSMAN	

F I G. 22



APPROVED BY DRAFTSMAN	O.G. FIG. CLASS      SUBCLASS
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FIG. 23A

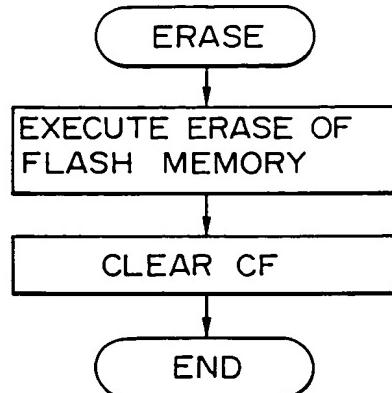


FIG. 23B

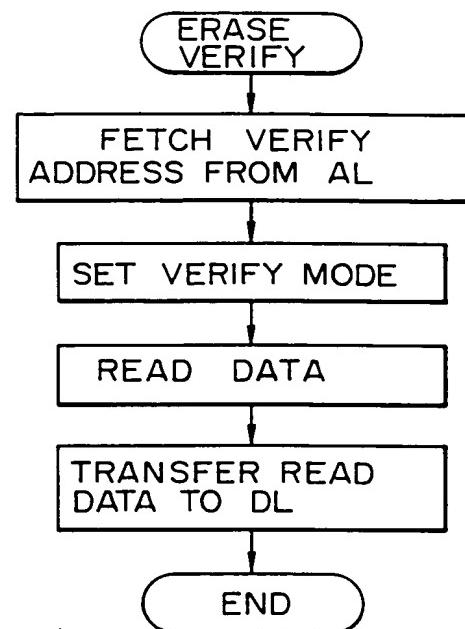


FIG. 24

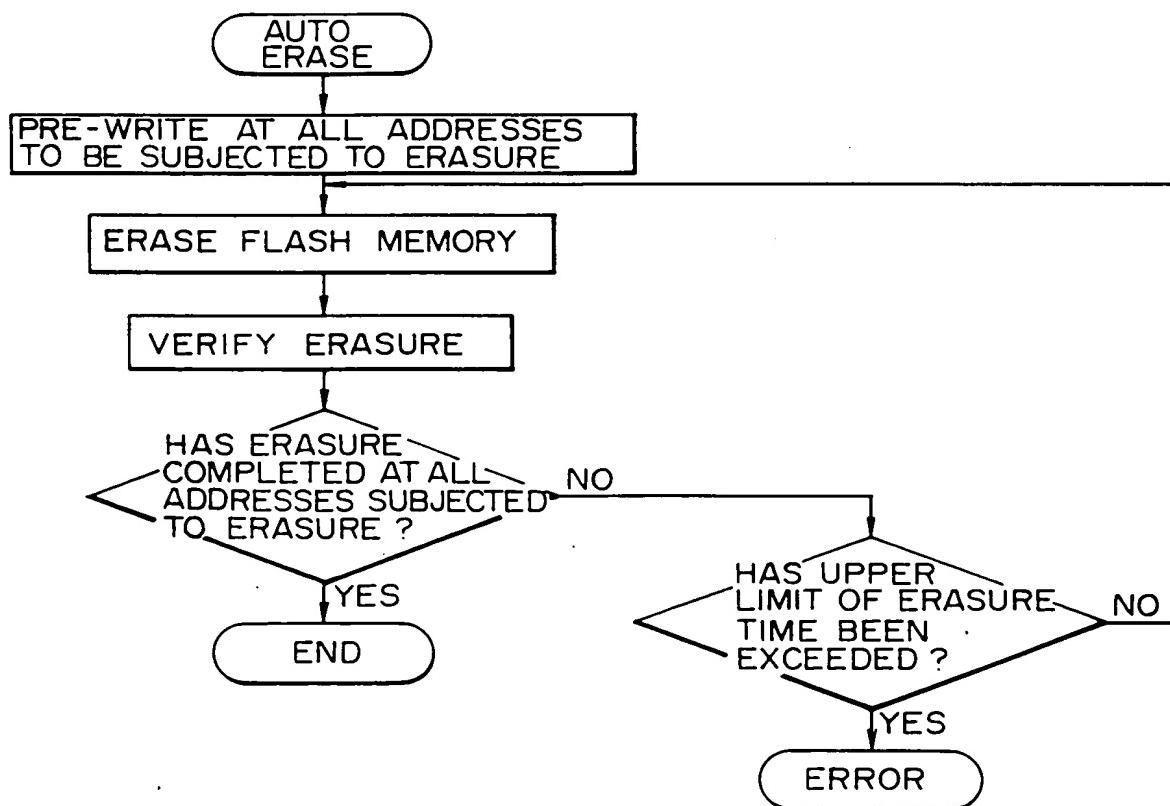
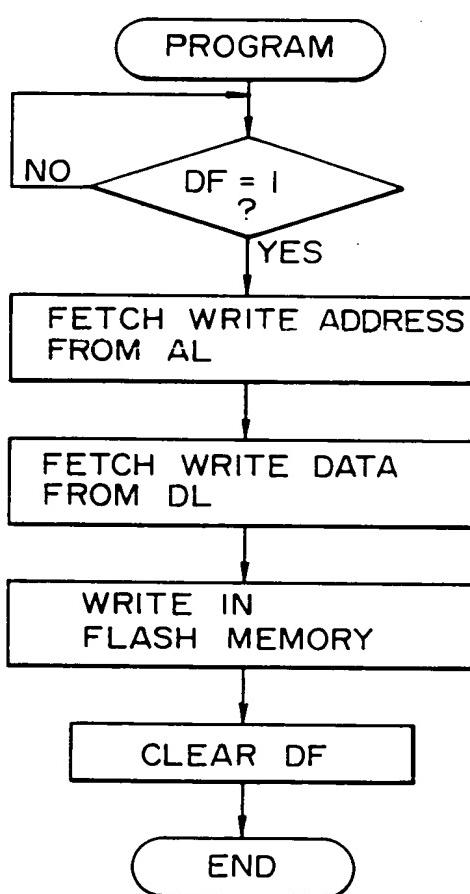
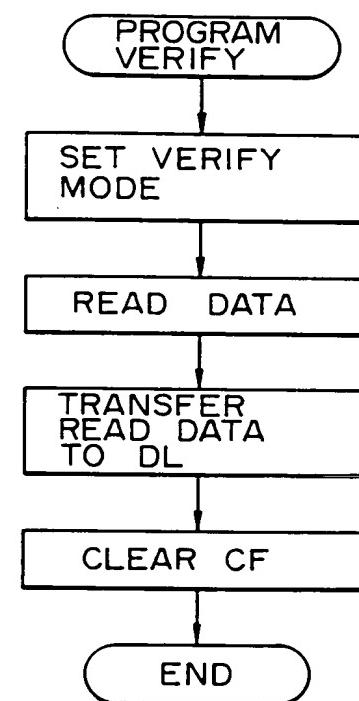


FIG. 25 A



**F I G. 25 B**



ପ୍ରକାଶକ ପତ୍ର ପରିଚୟ